**Encoder & Decoder**

**Lab no #06**

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**CSE Digital logic and computer design**

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Registration No.: **20pwcse1952**

Class Section: **C**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Submitted to: Sir Faiz ullah

12/14/2021

**Department of Computer Systems Engineering**

**University of Engineering and Technology, Peshawar**

**OBJECTIVES:**

After completing this experiment, you will be able to:

* Design and construct Decoder and Encoder
* Verify their truth tables using logic gates

**COMPONENTS REQUIRED:**

 Two 7410, 3 I/P NAND gate

 Three 7432, 2 I/P OR gate

 7404 hex inverters

**THEORY:**

**DECODER:**

A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, but we will begin our study of encoders and decoders with decoders because they are simpler to design. A decoder is a device that generates the original signal as output from the coded input signal and converts n lines of input into 2n lines of output. An AND gate can be used as the basic decoding element because it produces a high output only when all inputs are high.

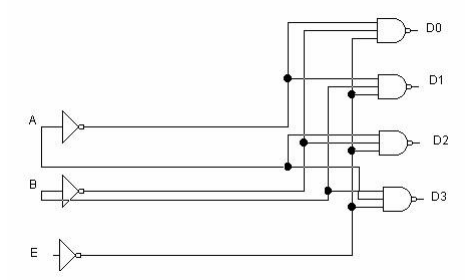
**ENCODER:**

An **Encoder** is a combinational circuit that performs the reverse operation of Decoder. It has maximum of 2n input lines and ‘n’ output lines. It will produce a binary code equivalent to the input, which is active High. Therefore, the encoder encodes 2n input lines with ‘n’ bits. It is optional to represent the enable signal in encoders. Simply put, an encoder is a sensing device that provides feedback. Encoders convert motion to an electrical signal that can be read by some type of control device in a motion control system, such as a counter or PLC. The encoder sends a feedback signal that can be used to determine position, count, speed, or direction.

**PROCEDURE:**

* Connections are given as per circuit diagram.
* Logical inputs are given as per circuit diagram.
* Observe the output and verify the truth table.

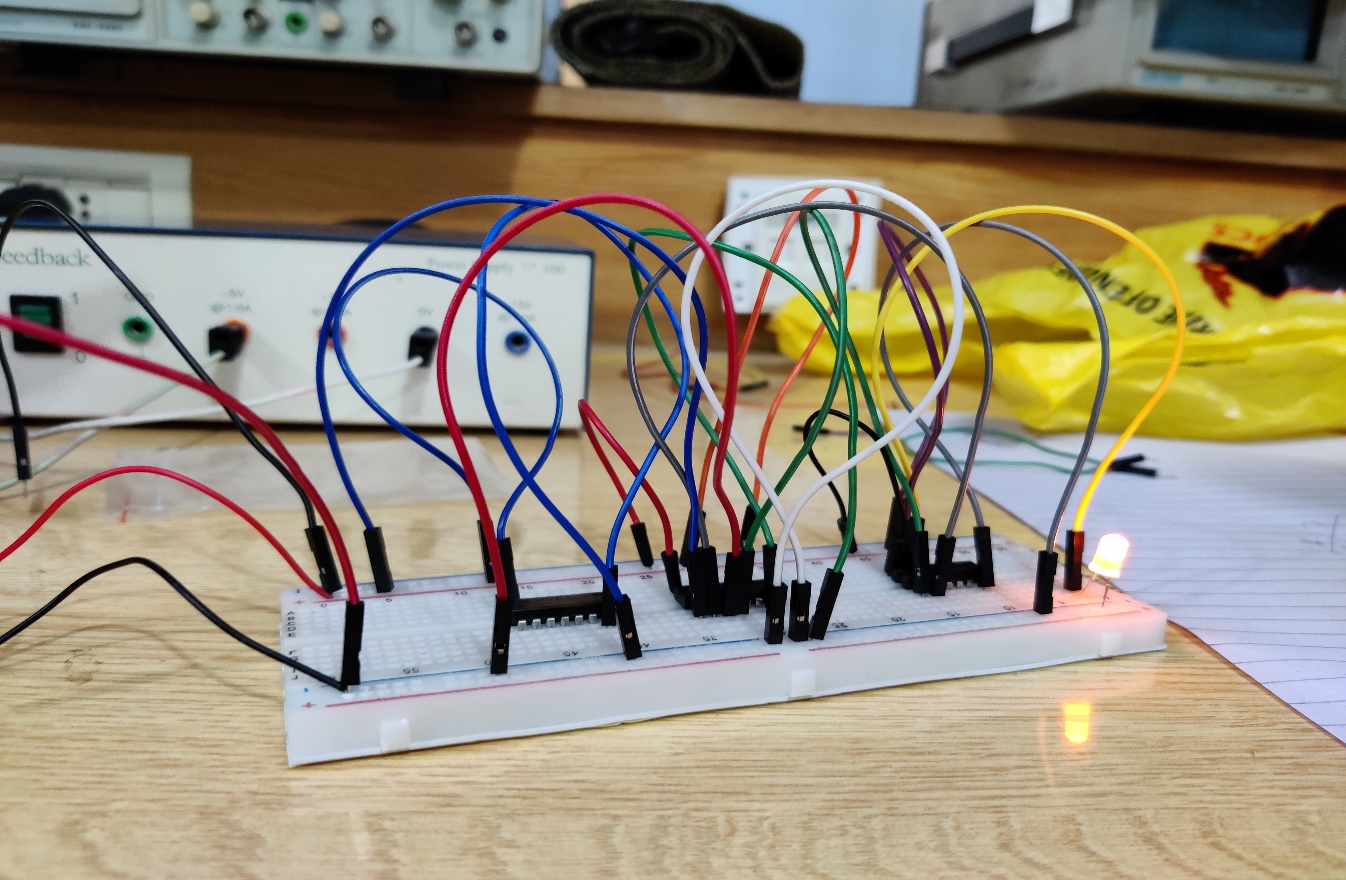
**LOGIC DIAGRAM FOR DECODER**



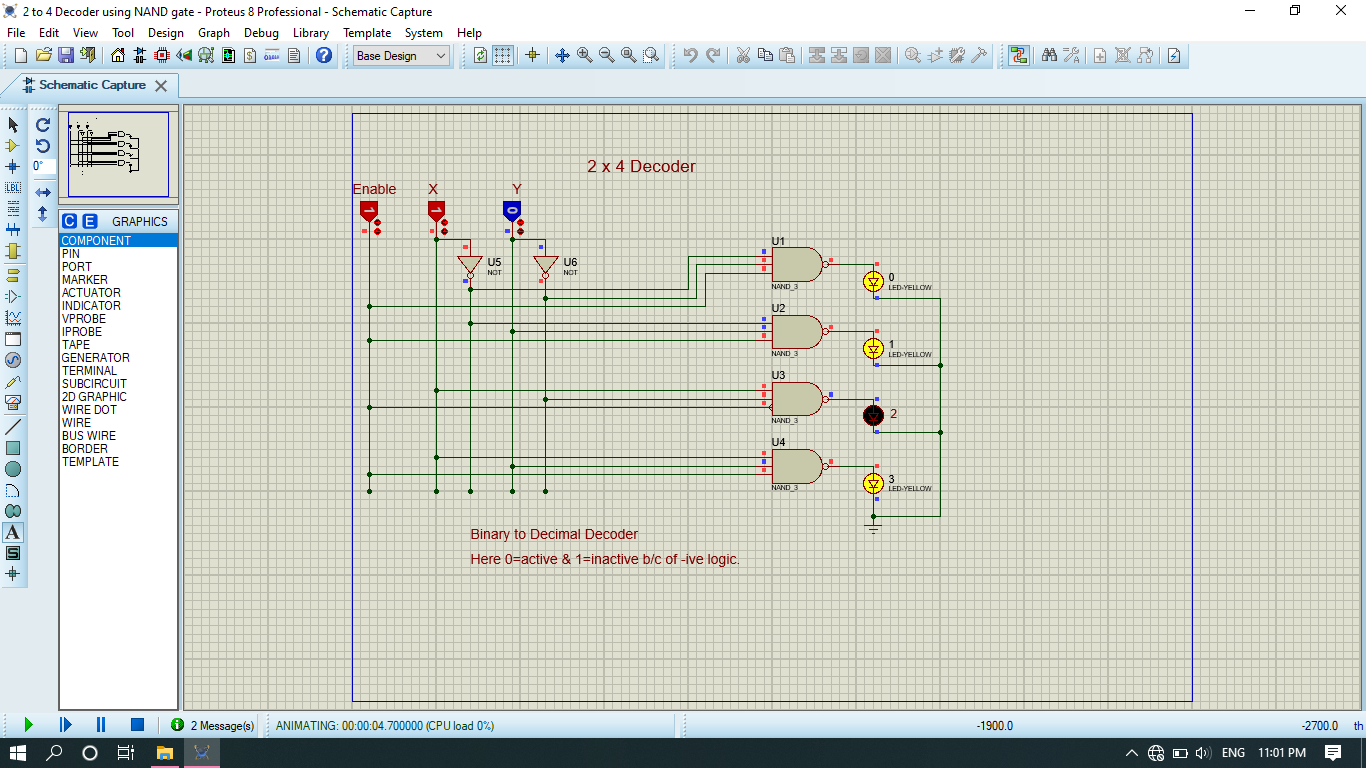
**Truth table:**

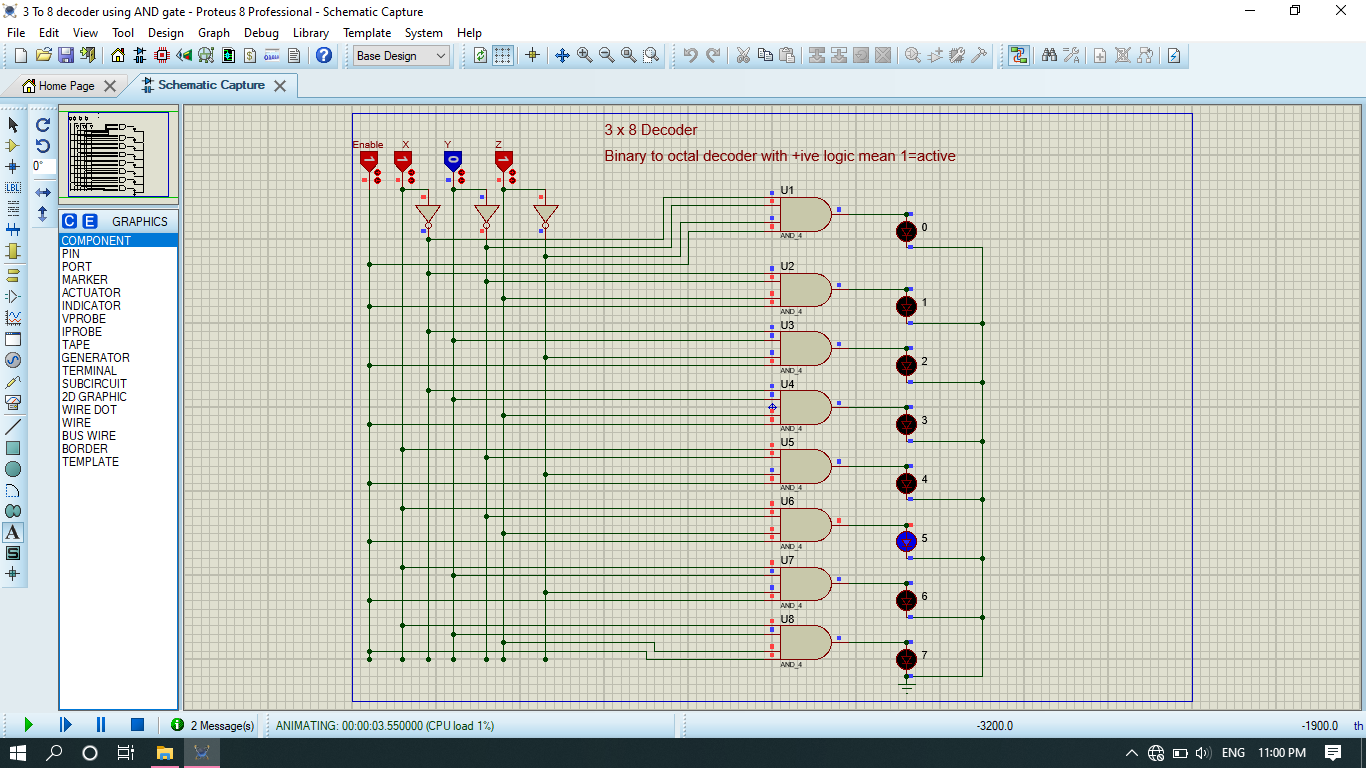
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **input** | | | **output** | | | |
| **E** | **A** | **B** | **D0** | **D1** | **D2** | **D3** |
| **1** | **x** | **x** |  |  |  |  |
| **0** | **0** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **1** | **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** | **1** | **0** |

**Real life circuit:**

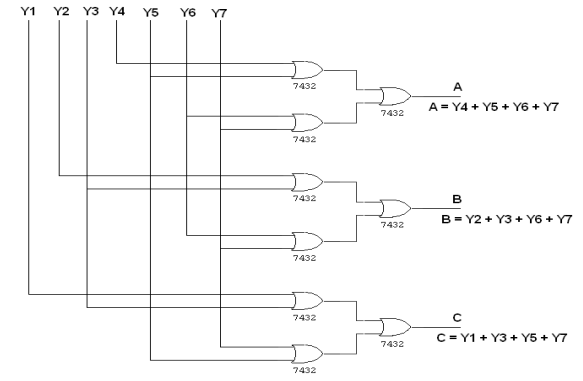


Proteus pic:

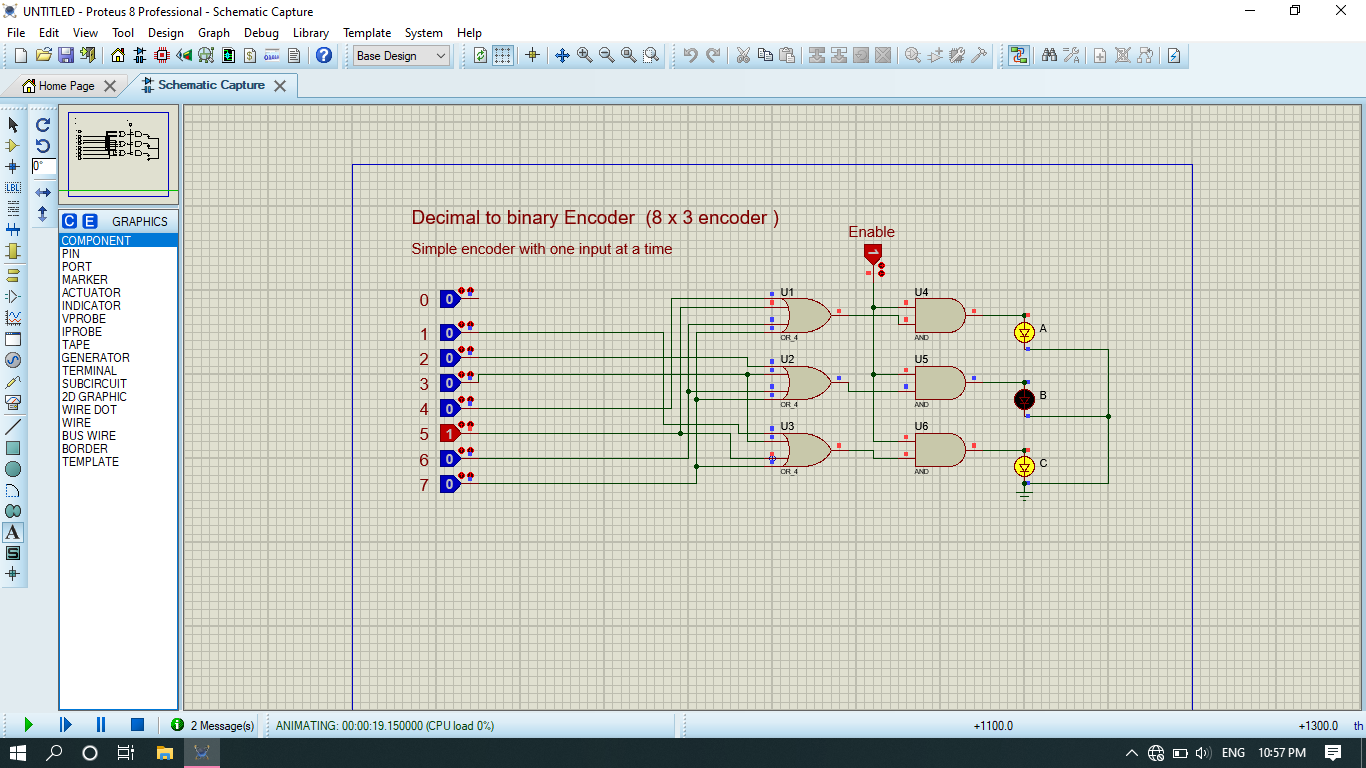


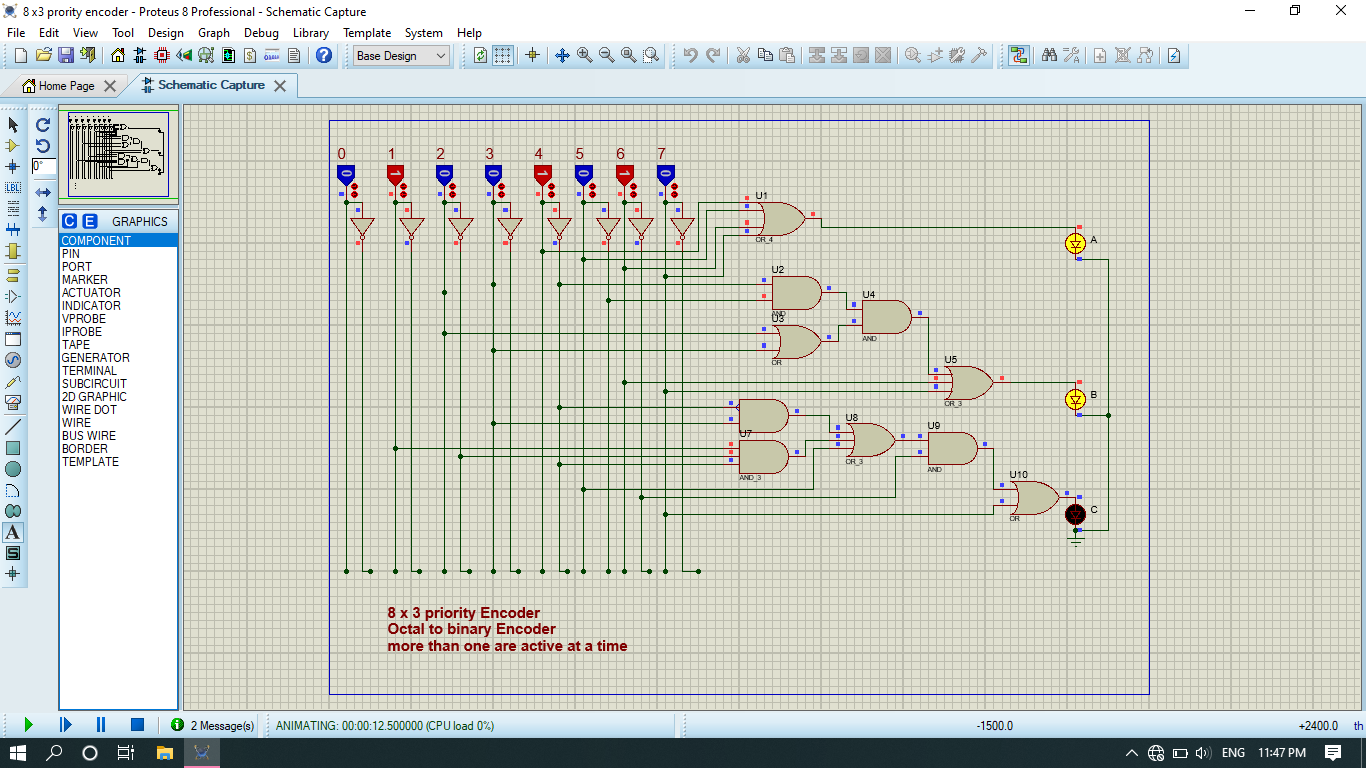


**LOGIC DIAGRAM FOR ENCODER**



Proteus pic:



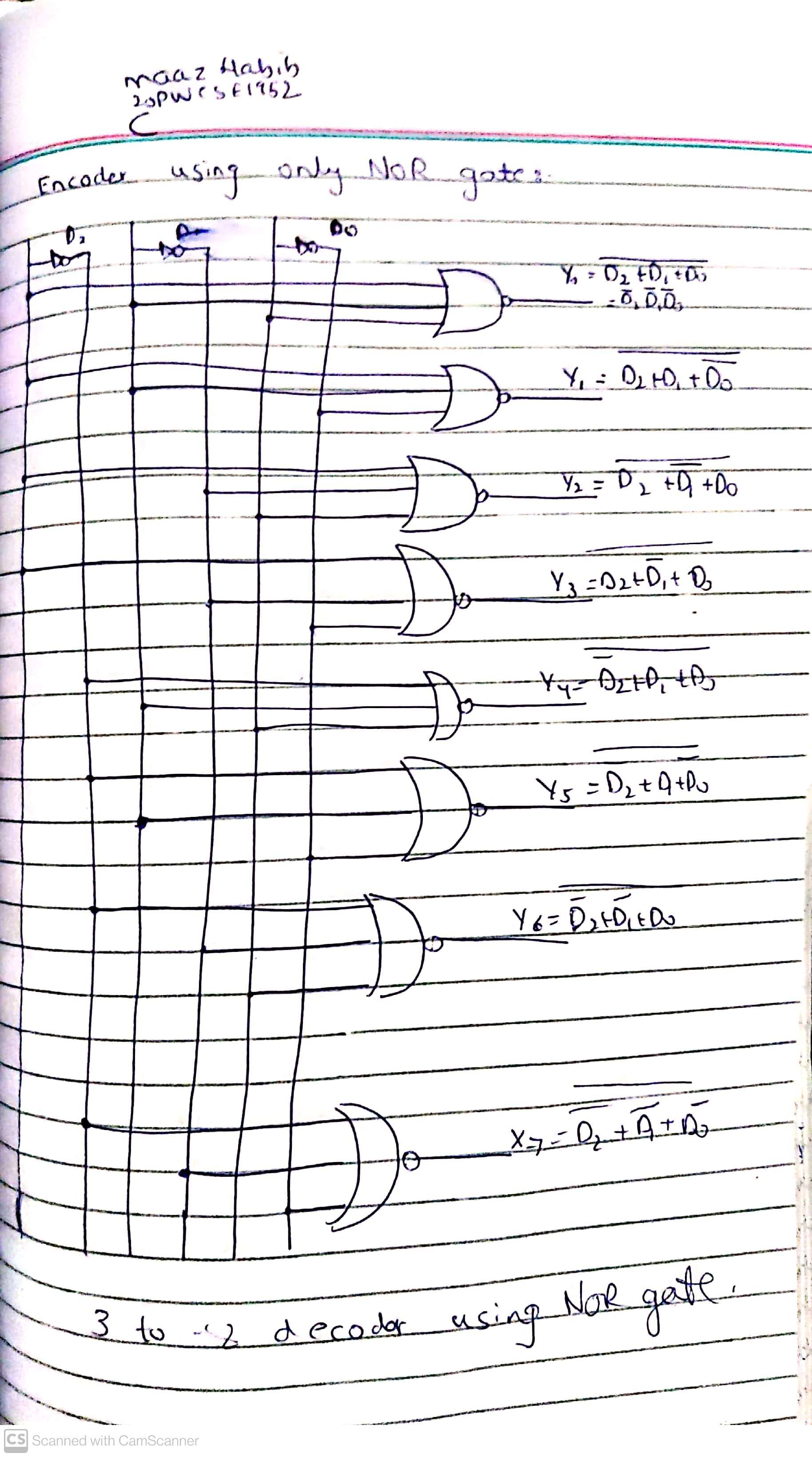


**TRUTH TABLE**

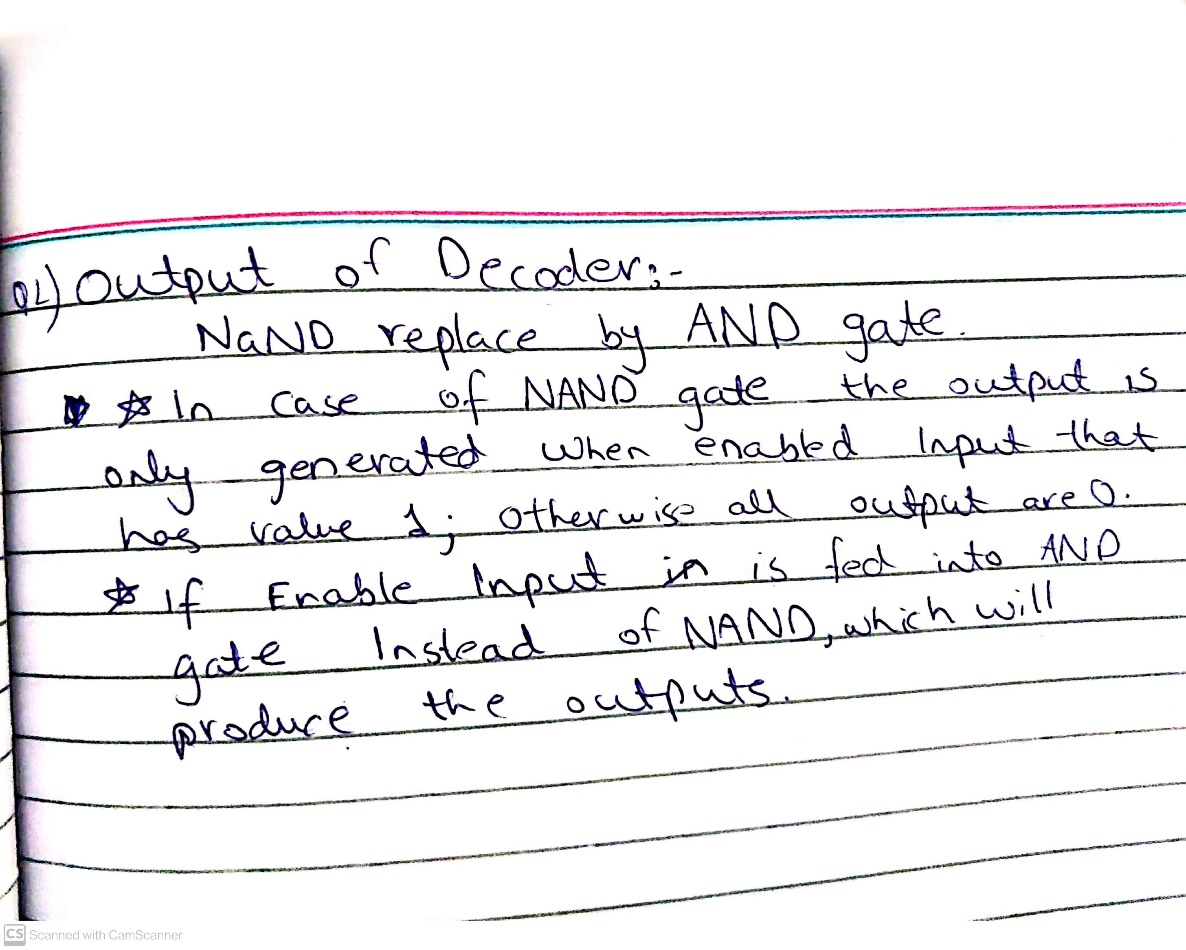
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **input** | | | | | | |  | **output** | | |
| **Y1** | **Y2** | **Y3** | **Y4** | **Y5** | **Y6** | **Y7** | **Y8** | **A** | **B** | **C** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** |

**REVIEW QUESTIONS**

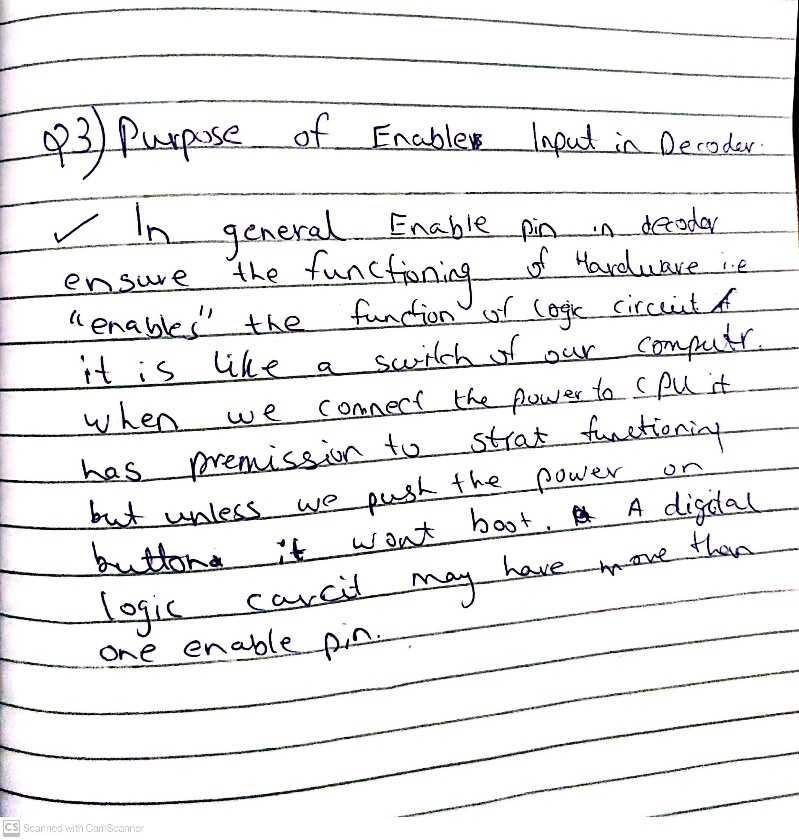
**Question no 1:**



**Question no 2:**



**Question no 3:**

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**Question no 4:**

